Introduction

The Xilinx® LogiCORE™ IP Accumulator core provides LUT and single XtremeDSP™ slice accumulation implementations. The Accumulator module can generate adder-based, subtracter-based and adder/subtracter-based accumulators operating on signed or unsigned data. The function can be implemented in a single XtremeDSP slice or LUTs (but currently not a hybrid of both). Pipelining is available for both implementations.

Features

- Drop-in module for Virtex®-7 and Kintex™-7, Virtex-6, Virtex-5, Virtex-4, Spartan®-6, Spartan-3/XA, Spartan-3E/XA, Spartan-3A/3AN/3A DSP/XA FPGAs

- Backwards compatible with version 9.1

- Generates add, subtract, and add/subtract-based accumulators

- Supports two's complement signed and unsigned operations

- Supports fabric implementation outputs up to 256 bits wide

- Supports XtremeDSP slice implementation outputs up to 48 bits wide (max width varies with device family)

- Supports pipelining (automatic and manual)

- User programmable feedback scaling for fabric implementations

- Optional carry output

- Optional clock enable and sclr

- Optional Bypass (Load) capability

- For use with the Xilinx CORE Generator™ tool and Xilinx System Generator for DSP 13.1

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family[1]			Virtex-7 and Kintex-7, Virtex-6, Virtex-5, Virtex-4, Spartan-6, Spartan-3/XA, Spartan-3E/XA, Spartan-3A/3AN/3A DSP/XA		
Supported User Interfaces			Not Applicable		
	Resources[2]				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Virtex-5, 32-bit output, add only	32	32	0	0	445 MHz
Provided with Core					
Documentation			Product Specification		
Design Files			Netlist		
Example Design			Not Provided		
Test Bench			Not Provided		
Constraints File			Not Applicable		
Simulation Model			VHDL behavioral model in the xilinxcorelib library VHDL UniSim structural model Verilog UniSim structural model		
Tested Design Tools					
Design Entry Tools			CORE Generator tool 13.1 System Generator for DSP 13.1		
Simulation			Mentor Graphics ModelSim 6.6d Cadence Incisive Enterprise Simulator (IES) 10.2 Synopsys VCS and VCS MX 2010.06 ISIM 13.1		
Synthesis Tools			N/A		
Support					
Provided by Xilinx, Inc.					

1. For the complete list of supported devices, see the release notes for this core.
2. For more complete performance data, see "Performance and Resource Utilization," page 6
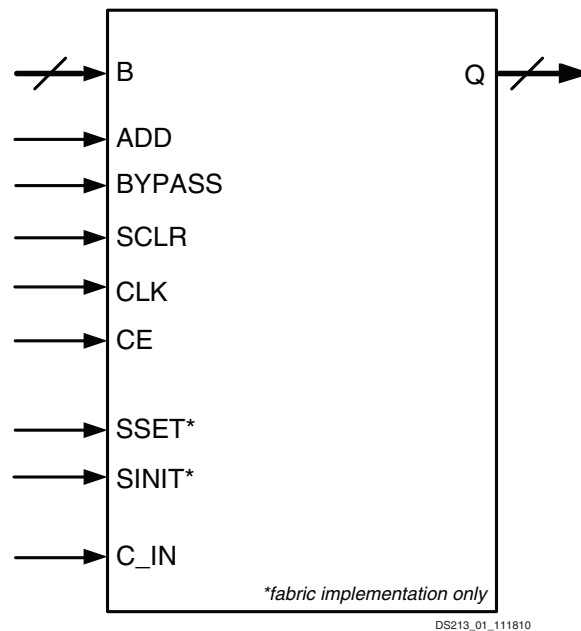
Pinout

Figure 1: **Core Symbol**

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1. Note that Figure 1 shows the SSET and SINIT pins which appear only on fabric implementations. The XtremeDSP slice implementations do not support SSET and SINIT.

Table 1: **Core Signal Pinout**

Name	Direction	Description
B[M:0]	Input	Input bus
ADD	Input	Controls operation performed by Adder/Subtractor-based accumulator (High = Addition, Low = Subtraction)
Q[P:0]	Output	Output bus
BYPASS	Input	Enables the value on port B to bypass the accumulator logic and appear directly on the output register (optionally active low)
CE	Input	Active high Clock Enable
CLK	Input	Clock signal: rising edge
SCLR	Input	Synchronous Clear: forces the output to a low state when driven high
SINIT[1]	Input	Synchronous Initialize: forces outputs to user defined state when driven high
SSET[1]	Input	Synchronous Set: forces the output to a high state when driven high
C_IN	Input	Carry Input

1. Available only for **Implement using** = Fabric

CORE Generator Software Graphical User Interface Parameters

The CORE Generator software GUI parameters for this module are described in the following items:

- **Implement using**: Sets the implementation type: Fabric or DSP48.

- **Input Width**: Sets the width of the input port.

- **Input Type**: Sets the type of the Port B data: Signed or Unsigned.

- **Output Width**: Sets the output width.

- **Accumulation Mode**: Sets the mode of operation of the module. If an adder/subtracter is specified, the ADD pin sets the mode of operation.

- **Carry In**: When set to true, this generic creates port C_IN which is the synchronous carry-in to the accumulator.

- **Bypass**: When set to true, creates a BYPASS pin. Activating the BYPASS pin sets the output to be the value given on Port B. This functionality is used for creating loadable accumulators.

- **Bypass Sense**: When set to Active Low, the BYPASS pin is active low. BYPASS is the only pin that has a parameter to control its active sense. This is because an historical implementation made significant speed gains with an active-low BYPASS, instead of active-high BYPASS. This is no longer necessarily the case, as sometimes active-high is as efficient, or more so. The details depend on the exact set of parameters.

- **Accumulator Scaling**: Sets the scaling factor used for the feedback path to Port B on fabric implementations. The value represents the number of low-order bits that are discarded in the feedback process.

- **Clock Enable**: When set to true, the module is generated with a clock enable input.

- **Power-on Reset Init value**: Specifies in binary the value the output initializes to during power-up reset.

- **Synchronous Clear**: Specifies if an SCLR pin is to be included.

- **Synchronous Set**: Specifies if an SSET pin is to be included. SSET pin is not valid in DSP48 implementations. See **Sync Set and Clear (Reset) Priority** for SCLR/SSET priorities.

- **Synchronous Init**: Specifies if an SINIT pin is to be included which, when asserted, synchronously sets the output value to the value defined by **Init Value**. Note that if SINIT is present, then neither SSET nor SCLR may be present. The SINIT pin is not valid in DSP48 implementations.

- **Init Value**: Specifies, in hex, the value that the output initializes to when SINIT is asserted. Ignored if **Synchronous Init** = 0.

- **Synchronous Controls and Clock Enable (CE) Priority**: This parameter controls whether or not the SCLR (and if fabric: SSET and SINIT) inputs are qualified by CE. When set to Sync_Overrides_CE, the synchronous controls override the CE signal. When set to CE_Overrides_Sync, the control signals have an effect only when CE is high. Note that on the fabric primitives, the SCLR and SSET controls override CE, so choosing CE_Overrides_Sync generally results in extra logic.

- **Sync Set and Clear (Reset) Priority**: Controls the relative priority of SCLR and SSET. When set to Reset_Overrides_Set, SCLR overrides SSET. The default is Reset_Overrides_Set, as this is the way the primitives are arranged. Making SSET take priority requires extra logic.

- **Latency Configuration**: Automatic sets optimal latency for maximum speed; Manual allows user to set Latency to one of the allowed values.

- **Latency**: Value used for latency when `Latency Configuration` is set to Manual. See the section, "Pipelined Operation", for more information.

Table 2 is a cross-reference table from the GUI parameters listed above to the XCO parameter names in the XCO file.

Table 2: **CORE Generator Tool GUI and XCO Parameters**

GUI Name	Default Value	Valid Range	XCO Parameter
Component Name	Accumulator		component_name
Implement using	Fabric		Implementation
Input Type	Signed		Input_Type
Input Width	16	1 to 255 (unsigned fabric) 2 to 256 (signed fabric) 1 to 47 (unsigned DSP48) 2 to 48 (signed DSP48)	Input_Width
Output Width	16	**Input Width** to 257 (unsigned fabric) **Input Width** to 258 (signed fabric **Input Width** to 47 (unsigned DSP48) **Input Width** to 48 (signed DSP48)	Output_Width
Latency Configuration	Manual		Latency_Configuration
Latency	1	1 to min of **Output Width** and 32 (Fabric) 1, 2 (DSP48)	Latency
Clock Enable	false		CE
Synchronous Clear	false		SCLR
Synchronous Set	false		SSET
Synchronous Init	false		SINIT
Bypass	true		Bypass
Bypass Sense	Active_High		Bypass_Sense
Carry In	false		C_In
Accumulation Mode	Add	Add, Subtract, Add_Subtract	Accum_Mode
Accumulator Scaling	0	0 to 8	B_Constant
Sync Set and Clear (Reset) Priority	Reset_Overrides_Set		SyncCtrlPriority
Synchronous Controls and Clock Enable (CE) Priority	Sync_Overrides_CE		Sync_CE_Priority
Power-on Reset Init Value	0	0 to $2^{\textbf{Output Width}} - 1$	AINIT_Value
Init Value	0	0 to $2^{\textbf{Output Width}} - 1$	SINIT_Value

Core Use through CORE Generator Tool

The CORE Generator software GUI performs error-checking on all input parameters. Resource estimation and latency information are also available.

Several files are produced when a core is generated, and customized instantiation templates for Verilog and VHDL design flows are provided in the .veo and .vho files, respectively. For detailed instructions, see the CORE Generator software documentation.

Simulation Models

The core has a number of options for simulation models:

- VHDL behavioral model in the xilinxcorelib library
- VHDL UniSim structural model
- Verilog UniSim structural model

Xilinx recommends that simulations utilizing UniSim-based structural models are run using a resolution of 1 ps. Some Xilinx library components require a 1 ps resolution to work properly in either functional or timing simulation. The UniSim-based structural models might produce incorrect results if simulation with a resolution other than 1 ps. See the "Register Transfer Level (RTL) Simulation Using Xilinx Libraries" section in *Synthesis and Simulation Design Guide* for more information. This document is part of the ISE® Software Manuals set available at www.xilinx.com/support/software_manuals.htm.

Core Use through System Generator

The Accumulator core is available through Xilinx System Generator for DSP, a DSP design tool that enables the use of the model-based design environment Simulink® software for FPGA design. The Accumulator core is one of the DSP building blocks provided in the Xilinx DSP blockset for the Simulink software. The core may be found in the Xilinx Blockset in the Math section. The block is called "Accumulator". See the System Generator for DSP User Guide for more information.

Migrating to Accumulator v11.0 from Earlier Versions

Updating from Accumulator v9.0 and Later

The CORE Generator core update feature may be used to update an existing Accumulator XCO file to version 11.0 of the core. The core may then be regenerated to create a new netlist. See the CORE Generator documentation for more information on this feature.

Updating from Versions Prior to Accumulator v9.0

It is not currently possible to automatically update versions of the Accumulator core prior to v9.0. Xilinx recommends that customers use the Accumulator v11.0 GUI to customize a new core. Note that some features and configurations may be unavailable in Accumulator v11.0. Also, some port names may differ between versions.

Pipelined Operation

The Accumulator module can be optionally pipelined to improve speed. The pipelined operation is controlled by the latency parameters. Set **Latency Configuration** to Automatic to achieve optimal pipelining for maximum speed. Set **Latency Configuration** to Manual to allow a valid number of pipeline stages to be entered in the **Latency** parameter. For **Latency** = 1, only output registers will be present. For **Latency** = 2, output and input registers will be present.

After power up or reset, the pipelined module takes a number of clock cycles, specified by the latency control, for the outputs to become valid.

If **Bypass** is requested on a pipelined module, the BYPASS input appears on the output after the number of clock cycles, specified by the latency control.

Performance and Resource Utilization

Tables 3 to 6 provide Accumulator performance and resource usage for a number of different Accumulator configurations.

The maximum clock frequency results were obtained by double-registering input and output ports to reduce dependence on I/O placement. The inner level of registers used a separate clock signal to measure the path from the input registers to the first output register through the core.

The resource usage results do not include the above "characterization wrapper" registers and represent only the logic used by the core. LUT counts include SRL16s or SRL32s (according to device family).

The map options used were: "map -pr b -ol high."

The par options used were: "par -ol high."

Clock frequency does not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification.

The maximum achievable clock frequency and the resource counts may also be affected by other tool options, additional logic in the FPGA device, using a different version of Xilinx tools, and other factors. The Xilinx Xplorer™ script can be used to find the optimal settings.

All characterization was done using the following parameter settings unless otherwise noted:

- **Input Width** = 1/2 **Output Width**
- **Clock Enable** = true
- **Bypass** = false unless otherwise noted
- **Input Type** = Signed
- **Latency Configuration** = Automatic
- **Accumulation Mode** = Add/Add_Subtract; the results in the characterization tables display these two accumulation modes as value/value.

Table 3: **Fabric Accumulator: Virtex-5 FPGA (Part = XC5VSX50T-1)**

Description	Non-Pipelined				Pipelined				
Output Width	8	32	64	100	8	32	64	100	64
Bypass	no	no	no	no	no	no	no	no	yes
Max Clock Frequency (MHz)	452/452 [1]	445/366	324/290	235/227	452/452	452/388	452/347	452/310	452/332
LUT6-FF pairs	8/8	32/32	64/64	100/100	8/8	74/145	221/364	395/630	226/368
LUTs	8/8	32/32	64/64	100/100	8/8	36/105	118/257	240/461	118/258
Flip-flops	8/8	32/32	64/64	100/100	8/8	73/76	217/228	387/402	222/232
DSP48Es	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0

1. All values in table are Add/Add_Subtract for **Accumulation Mode**.

Table 4: **XtremeDSP Slice Accumulator: Virtex-5 FPGA (Part = XC5VSX50T-1)**

Description	Non-Pipelined	Pipelined			
Output Width	32	8	32	48	32
Bypass	no	no	no	no	yes
Clock Frequency (MHz)	360/353 [1]	445/445	445/445	445/445	445/445
LUT6-FF pairs	0/0	0/0	0/0	0/0	0/1
LUTs	0/0	0/0	0/0	0/0	0/1
Flip-flops	0/0	0/0	0/0	0/0	0/0
DSP48Es	1/1	1/1	1/1	1/1	1/1

1. All values in table are Add/Add_Subtract for **Accumulation Mode**.

Table 5: **Fabric Accumulator: Spartan-3A DSP FPGA (Part = XC3SD3400A-4)**

Description	Non-Pipelined				Pipelined				
Output Width	8	32	64	100	8	32	64	100	64
Bypass	no	no	no	no	no	no	no	no	yes
Max Clock Frequency (MHz)	251/251 [1]	188/188	125/125	102/94	251/251	244/180	236/172	212/165	228/165
LUTs	8/8	32/32	64/64	100/100	8/8	38/108	142/284	305/529	142/286
Flip-flops	8/8	32/32	64/64	100/100	8/8	93/96	241/248	419/436	248/255
DSP48As	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0

1. All values in table are Add/Add_Subtract for **Accumulation Mode**.

Table 6: **XtremeDSP Slice Accumulator: Spartan-3A DSP FPGA (Part = XC3SD3400A-4)**

Description	Non-Pipelined	Pipelined			
Output Width	32	8	32	48	32
Bypass	no	no	no	no	yes
Clock Frequency (MHz)	10/110 [1]	251/251	251/251	251/251	251/251
LUTs	0/1	0/1	0/1	0/1	1/1
Flip-flops	0/0	0/0	0/0	0/0	0/0
DSP48As	1/1	1/1	1/1	1/1	1/1

1. All values in table are Add/Add_Subtract for **Accumulation Mode**.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Refer to the IP Release Notes Guide (XTP025) for further information on this core. There is a link to all the DSP IP and then to each core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for each core. The following information is listed for each version of the core:

• New Features

• Bug Fixes

• Known Issues

Ordering Information

This LogiCORE IP module is included at no additional cost with the Xilinx ISE Design Suite software and is provided under the terms of the Xilinx End User License Agreement. Use the CORE Generator software included with the ISE Design Suite to generate the core. For more information, please visit the core page.

Please contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

Revision History

Date	Version	Description of Revisions
4/28/05	8.0	Updated to ISE Tools 7.1
4/24/09	11.0	Initial release of Accumulator core with XtremeDSP slice implementations and support for Virtex-6 and Spartan-6 devices
03/01/11	11.1	Support added for Virtex-7 and Kintex-7. ISE Design Suite 13.1

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